What is claimed is:

1. A transmitter comprising:

a first circuit coupled to an input port of the transmitter; and

a second circuit coupled to the first circuit and to an output port of the transmitter, wherein the first circuit is sized with respect to the second circuit such that for a pulse signal applied to the input port, the transmitter generates an output signal having a rise-time and a fall-time that are substantially equal at the output port.

2. The transmitter of claim 1, wherein the first circuit includes an inverter.

3. The transmitter of claim 2, wherein the inverter includes a *n*-type metal-oxide semiconductor field-effect transistor connected in series with an *p*-type metal-oxide semiconductor field-effect transistor.

4. The transmitter of claim 3, wherein the *n*-type metal-oxide semiconductor field-effect transistor is larger than the *p*-type metal-oxide semiconductor field-effect transistor.

5. The transmitter of claim 3, wherein the *n*-type metal-oxide semiconductor field-effect transistor is between about two and about three times larger than the *p*-type metal-oxide semiconductor field-effect transistor.

6. The transmitter of claim 1, wherein the second circuit includes a plurality of driver circuits.

7. The transmitter of claim 6, wherein each of the plurality of driver circuits includes a *p*-type metal-oxide semiconductor field-effect transistor connected in series with an *n*-type metal-oxide semiconductor field-effect transistor.

8. The transmitter of claim 7, wherein the *p*-type metal-oxide semiconductor field-effect transistor is sized to source a first current and the *n*-type metal-oxide semiconductor field effect transistor is sized to sink a second current substantially equal to the first current.

9. The transmitter of claim 7, wherein the second circuit is connected to an equalization control circuit.

10. The transmitter of claim 9, wherein the equalization control circuit provides de-emphasis.

11. The transmitter of claim 1, wherein the transmitter transmits at a signal level and the first circuit and the second circuit are coupled to a supply potential having a value of about twice the signal level.

12. A method comprising:

receiving a signal at a first circuit;

in a second circuit coupled to the first circuit, the second circuit including a plurality of *p*-type metal-oxide semiconductor field-effect transistors, enabling the plurality of *p*-type metal-oxide semiconductor field-effect transistors to drive a transmission line; and

enabling less than the plurality of the *p*-type metal-oxide semiconductor field-effect transistors to drive the transmission line.

13. The method of claim 12, wherein receiving a signal at a first circuit includes receiving a digital signal.

14. The method of claim 13, wherein enabling the plurality of *p*-type metal-oxide semiconductor field-effect transistors to drive a transmission line includes enabling the plurality of *p*-type metal-oxide semiconductor field-effect transistors substantially simultaneously.

15. The method of claim 14, wherein enabling less than all of the *p*-type metal-oxide semiconductor field-effect transistors to drive the transmission line comprises enabling less than all of the *p*-type metal-oxide semiconductor field-effect transistors substantially simultaneously.

16. A system comprising:

a transmitter including:

a first circuit coupled to an input port of the transmitter; and

a second circuit to couple the first circuit to an output port of the transmitter, the second circuit coupled to an equalization control circuit;

a receiver; and

a transmission line to couple the output port of the transmitter to the receiver.

17. The system of claim 16, wherein the first circuit including an inverter having a *p*-type metal-oxide semiconductor field-effect transistor and an *n*-type metal oxide semiconductor field-effect transistor, the *n*-type metal-oxide semiconductor field-effect transistor being between about two and about three times larger than the *p*-type metal oxide semiconductor field-effect transistor.

18. The system of claim 17, wherein the second circuit includes a voltage driver.

19. The system of claim 18, wherein the second circuit includes a controllable source impedance.

20. A system comprising:

a first processor including a transmitter comprising:

a first circuit coupled to an input port of the transmitter; and

a second circuit coupled to the first circuit and to an output port of the transmitter, wherein the first circuit is sized with respect to the second circuit such that for a pulse signal applied to the input port, the transmitter generates an output signal having a rise-time and a fall-time that are substantially equal at the output port; and

a second processor including a receiver coupled to the transmitter through a transmission line.

21. The system of claim 20, wherein the first processor includes a very long instruction word processor.

22. The system of claim 21, wherein the second processor includes a complex instruction set processor.

23. The system of claim 22, further comprising an equalization control circuit coupled to the second circuit to provide de-emphasis equalization.